

IEEE 1149 Family

Carl F. Barnhart



2006 South-West Test Conference

Agenda

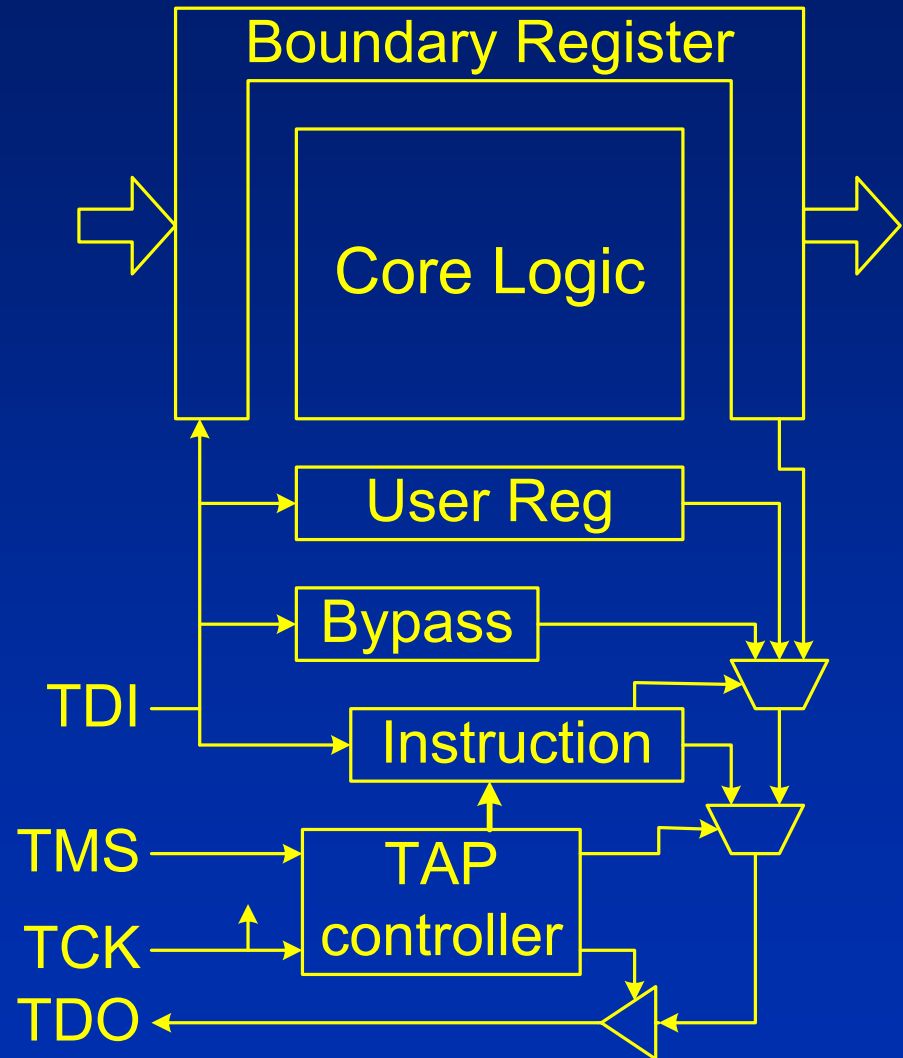
- Core capability: IEEE Standard 1149.1
- Enhancing Board Test:
 - IEEE Standard 1149.4: Analog nets
 - IEEE Standard 1149.6: Advanced I/O
- Internal Instrumentation: IEEE P1687
- System Level Protocol: IEEE Standard 1149.5
- 2-pin protocol with additional data transfer protocols: IEEE P1149.7

IEEE Standard 1149.1

- Intended for board test
 - Standard boundary register
 - Standard language (BSDL) to describe chip to board test without revealing internal design
- Included general test port capabilities:
 - Standard 4-5 pin Test Access Port (TAP)
 - Standard TAP Controller state machine for control
 - User defined instructions and test registers
 - Widely used for internal tests (MBIST, LBIST) and debug

IEEE 1149.1 Architecture

- Boundary Register and required instructions provide board test
- User Registers and Instructions provide general test access
- Single scan chain (TDI to TDO)



Tap Controller State Diagram

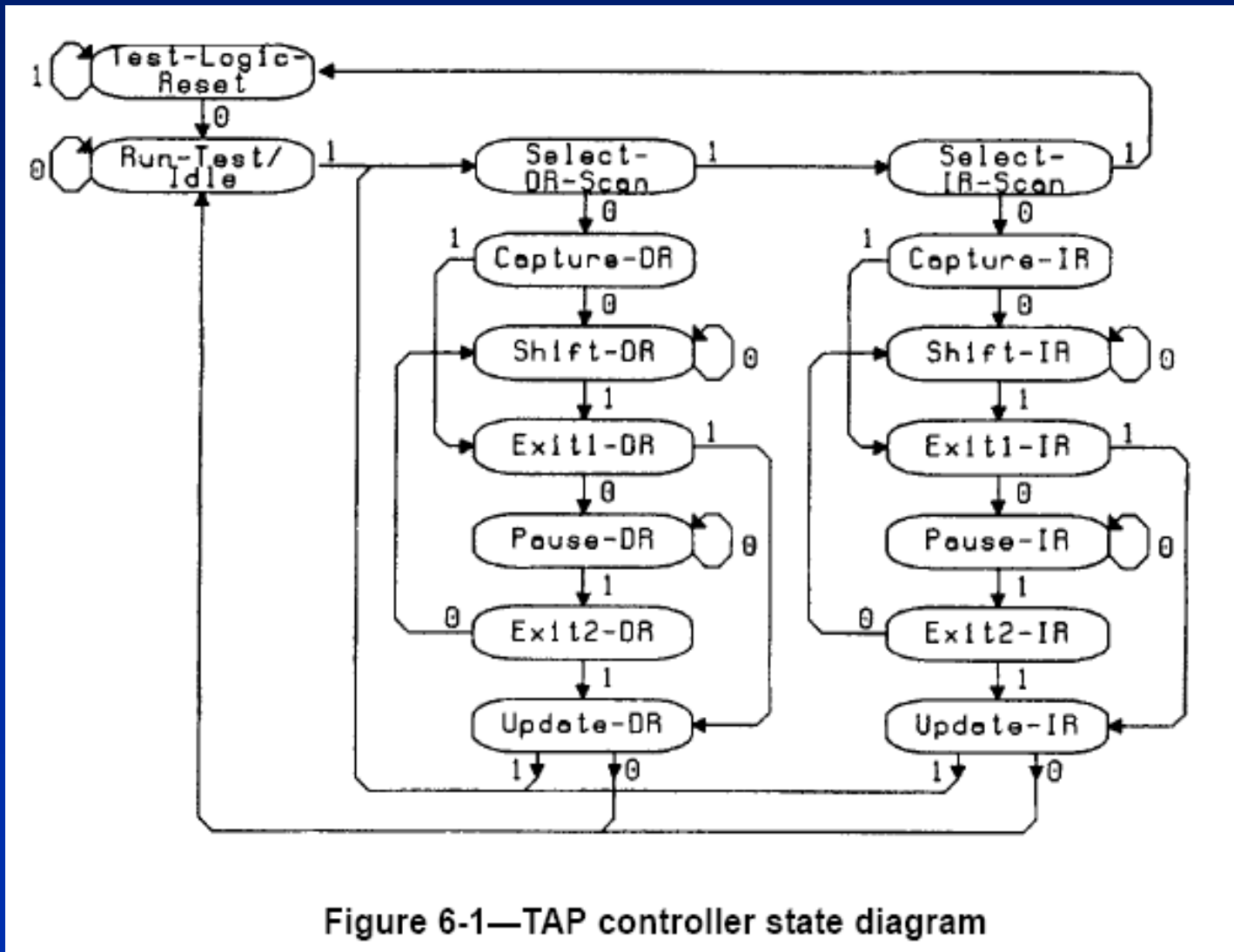


Figure 6-1—TAP controller state diagram

IEEE Standard 1149.4

- Adds ability to test analog interfaces including board level analog components
 - 2 added pins for analog test signals
 - Boundary register structures for routing analog test signals to selected analog pins
 - Analog instruments drive or receive through test pins to test selected paths
- Tests one path or component at a time
- Working on description language

IEEE Standard 1149.6

- Modern high-speed interfaces (such as SERDES) require capacitive coupling
- 1149.1 detects only about half the defects on differential channels
- New test receiver and other extensions permit detection of all defects on differential and AC-coupled nets
- Rapid adoption by industry

P1687 Proposed Standard

- Standardizes interface to internal test features (“instrumentation”)
 - Also known as iJTAG
 - Defines access and control protocols for instruments, not the instruments
 - Intends to use 1149.1 TAP for control
- Working group is active

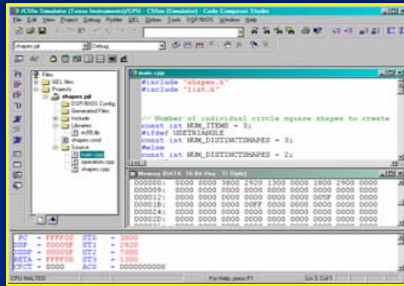
IEEE Standard 1149.5

- “System Level” protocol for control of multiple-board testing
- Usage not known...

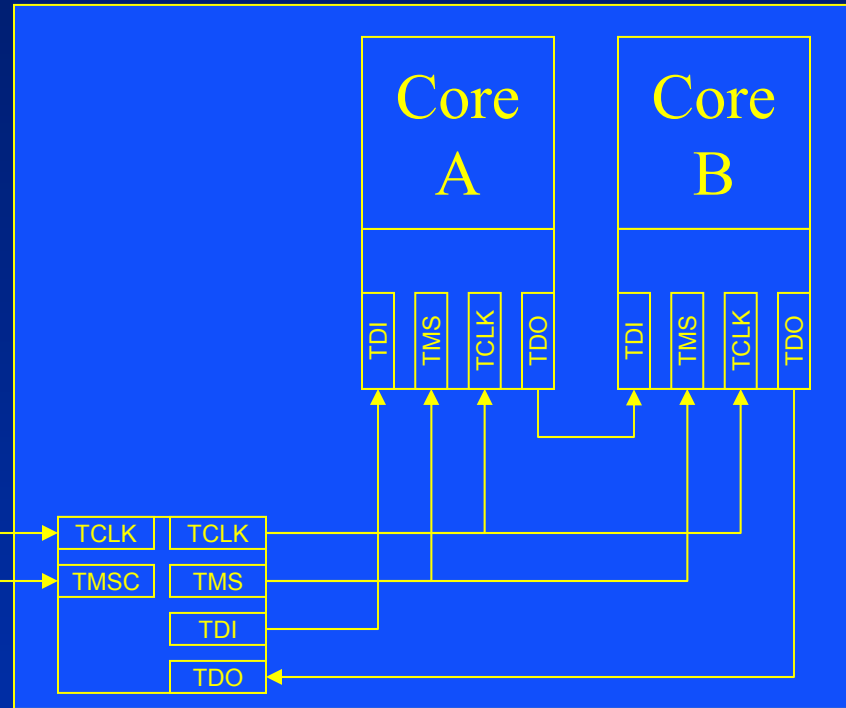
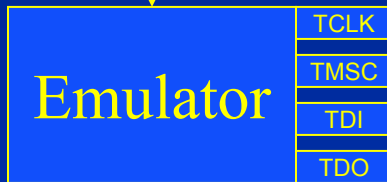
P1149.7 Proposed Standard

- Adds a new protocol layer on top of 1149.1
 - Preserves existing software and hardware
 - 2 pin interface in addition to 4-5 pin interface
 - Supports multiple TAPs on one chip
 - Multiple higher performance transfer protocols
- Provides more advanced system-level control
- Intended for small systems with limited I/O
but large SOC chips with many TAPs per chip

P1149.7 Architecture



SW Driver



•SW IP Preservation:

- Debugger tools
- SW Drivers

•Silicon IP Preservation:

- Compatible with existing Silicon IP
- Add at Chip Level

Pin use reduced in a compatible way!